Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A memory module, comprising:

a mounting ~~substrate; the mounting substrate having connections for supplying address and command signals,~~ substrate, wherein the substrate comprises connections for supplying address and command signals;

a plurality of integrated memory components~~, the components~~ arranged on the mounting ~~substrate;~~ substrate, wherein each of the memory components comprises a memory cell array including rows and columns;

a refresh control circuit~~, the refresh control circuit being~~ that is arranged separately from the memory components on the mounting substrate, ~~an output~~ wherein an output of the refresh control circuit ~~being~~ is connected to the plurality of integrated memory components and an input of the refresh control circuit is connected to the connections for supplying the address and command signals; and

~~the mounting substrate having connections for supplying address and command signals,~~

~~an input of the refresh control circuit being connected to the connections for supplying the address and command signals,~~

a respective set of counter circuits for independently operated units of rows, wherein the individual counter circuits within a set are associated with a respective different row in the corresponding unit of rows, and a respective counter circuit is reset when an associated row is accessed;

wherein the refresh control circuit ~~being~~ is designed such that[[,]]:

when address or command signals, which have been generated outside the memory module, are supplied, the refresh control circuit ~~receiving~~ receives and ~~processing~~ processes the signals, based on the access information obtained therefrom, the refresh control

circuit independently ~~generating~~ generates a refresh command for refreshing the contents of memory cells in a selected one of the memory components, and the refresh control circuit ~~transmitting~~ transmits the refresh command to the selected memory ~~component.~~ component; and

the refresh control circuit ascertains which rows in a selected memory component have not been accessed in a predefined period of time and, based on this evaluation, the refresh control circuit independently determines a point in time at which the refresh command will be sent, the refresh control circuit being configured to evaluate the counter circuits with respect to a count and, based on such evaluation, independently determining the point in time at which the refresh command will be sent.

2 - 6. (Canceled)

7. (Original) The memory module as claimed in claim 1, wherein the refresh control circuit is arranged within a semiconductor chip, the semiconductor chip being separate from the memory components.

8. (Original) The memory module as claimed in claim 1, wherein the input connection of the refresh control circuit is connected to a contact strip on the memory module.

9. (Original) The memory module as claimed in claim 1, wherein the memory module is in the form of a DIMM module arrangement.

10. (Original) The memory module as claimed in claim 1, wherein the memory components in the memory module are dynamic read/write memories.

11. (Currently Amended) A memory module, comprising:

a mounting ~~substrate; the mounting substrate having connections for supplying address and command signals,~~ substrate, wherein the substrate comprises connections for supplying address and command signals;

a plurality of integrated memory components~~, the components~~ arranged on the mounting ~~substrate;~~ substrate, wherein the memory components each comprises a memory cell array including rows and columns;

a refresh control circuit~~, the refresh control circuit being~~ that is arranged separately from the memory components on the mounting substrate, ~~an output~~ wherein an output of the refresh control circuit ~~being~~ is connected to the plurality of integrated memory components and an input of the refresh control circuit is connected to the connections for supplying the address and command signals; and

a respective set of counter circuits for independently operated units of rows, wherein the individual counter circuits within a set are associated with a respective different row in the corresponding unit of rows, and a respective counter circuit is reset when an associated row is accessed;

~~the mounting substrate having connections for supplying address and command signals,~~

~~an input of the refresh control circuit being connected to the connections for supplying the address and command signals,~~

wherein the refresh control circuit ~~being~~ is designed ~~such that,~~ such that:

when address or command signals, which have been generated outside the memory module, are supplied, the refresh control circuit ~~receiving~~ receives and ~~processing~~ processes the signals, based on the access information obtained therefrom, the refresh control circuit independently ~~generating~~ generates a refresh command sequence for refreshing the contents of memory cells in a selected one of the memory components, and the refresh control circuit ~~transmitting~~ transmits the command sequence to the selected memory ~~component.~~ component; and

the refresh control circuit ascertains which rows in a selected memory component have not been accessed in a predefined period of time and, based on this evaluation, the refresh control circuit independently determines a point in time at which the refresh command sequence will be sent, the refresh control circuit being configured to evaluate the counter circuits with respect to a count and, based on such evaluation, independently determining the point in time at which the refresh command sequence will be sent.

12 – 16. (Canceled)

17. (Original) The memory module as claimed in claim 11, wherein the refresh control circuit is arranged within a semiconductor chip, the semiconductor chip being separate from the memory components.

18. (Original) The memory module as claimed in claim 11, wherein the input connection of the refresh control circuit is connected to a contact strip on the memory module.

19. (Original) The memory module as claimed in claim 11, wherein the memory module is in the form of a DIMM module arrangement.

20. (Original) The memory module as claimed in claim 11wherein the memory components in the memory module are dynamic read/write memories.